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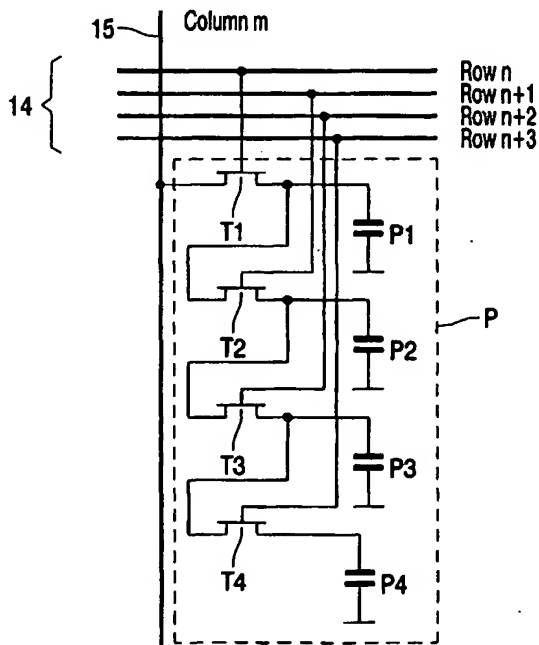
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(54) Title: ACTIVE MATRIX DISPLAY DEVICES



(57) Abstract: In an active matrix display device, such as an AMOLED, having an array of pixels (P) addressed via sets of row and column conductors (14, 15) to which, respectively, selection and data signals are applied, each pixel comprises a plurality of sub pixels (P1 - P4) which each have an associated switch, for example a TFT, (T1 - T4) and which are addressed with data signals through a common switch (T1) coupled to a column conductor (15). Addressing the sub pixels through a common switch reduces the effective capacitance of the column conductor. By appropriate control of the switches (T1 - T4) the pixels can be driven in a first mode in which the common switch (T1) is operated to control the simultaneous addressing of the sub pixels (P1 - P4) with a data signal, for example, for a video display with full grey scale capability, and in a second mode in which the switches (T1 - T4) are controlled sequentially to allow different data signals to be applied to the individual sub pixels, for example, as required for a low power standby mode of operation with limited grey scale and colour capability.

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